A2232 MULTIPORT SERIAL CARD
FUNCTIONAL SPECIFICATION

DESCRIPTION

The A2232 Multiport Serial Card is a standard 100 pin Zorro II expansion card for the Amiga 2000. It provides the Amiga with 7 additional standard RS232 serial ports, capable of speeds up to 19.2 kbaud. For more serial channels, additional A2232 boards can be plugged into the system at the same time.

SERIAL PORTS

All 7 of the serial ports are available at the rear of the board via 7 8-pin mini DIN connectors. The board comes with 7 short adapter cables which can be plugged into each of these connectors, which provides a more standard DB-25 connection.

signal	8 pin mini DIN	DB-25	dir
TxD / RxD	1	2	out/in
RxD / TxD	2	3	in/out
Request to Send (RTS)	3	4	out
Clear to Send (CTS)	4	5	in
Data Set Ready (DSR)	5	6	in
Signal Ground	6	7	
Data Carrier Detect (DCD)	7	8	in
Data Terminal Ready (DTR)	8	20	out

In order to simplify connections, the transmit data (TxD) and receive data (RxD) signals can be swapped on the A2232 board. There is an 8 jumper block (JB1) at the back of the board which makes this possible. Each of the 7 serial channels is associated with 4 possible jumper locations, and uses 2 of the jumpers. Figure 1 shows the schematic for this jumper block. Figure 2 shows how to configure the shorting blocks for a single channel.

All unused inputs have pullups on the board which keeps them at their 'TRUE' value if not connected. This greatly simplifies things if you are only using a 3-wire connection.

A2232 SYSTEM CONFIGURATION

The A2232 expansion card conforms to the auto-config protocol.

auto-config size	64k bytes
manufacturer code	202 (hex)
product number	46 (hex)

A block diagram of the board is shown in figure 3.

An 8 bit processor was incorporated in the A2232 in order to remove the burden of handling I/O from the Amiga system's main CPU. Also, since the Amiga is multi-tasking, it is impossible to ensure that the system's CPU can respond in a timely manner in order to service the needs of the I/O channels. The 8 bit processor used is a 65CE02, which is an enhanced version of the 6502, providing faster operation through new instructions and higher operating speeds.

The 6502 and the Amiga communicate mainly through the 16k bytes of shared RAM. The Amiga also has control over the 6502's *RESET and *IRQ signals. The 6502 can interrupt the Amiga via the *INT2 interrupt line. The Amiga must clear this interrupt itself.

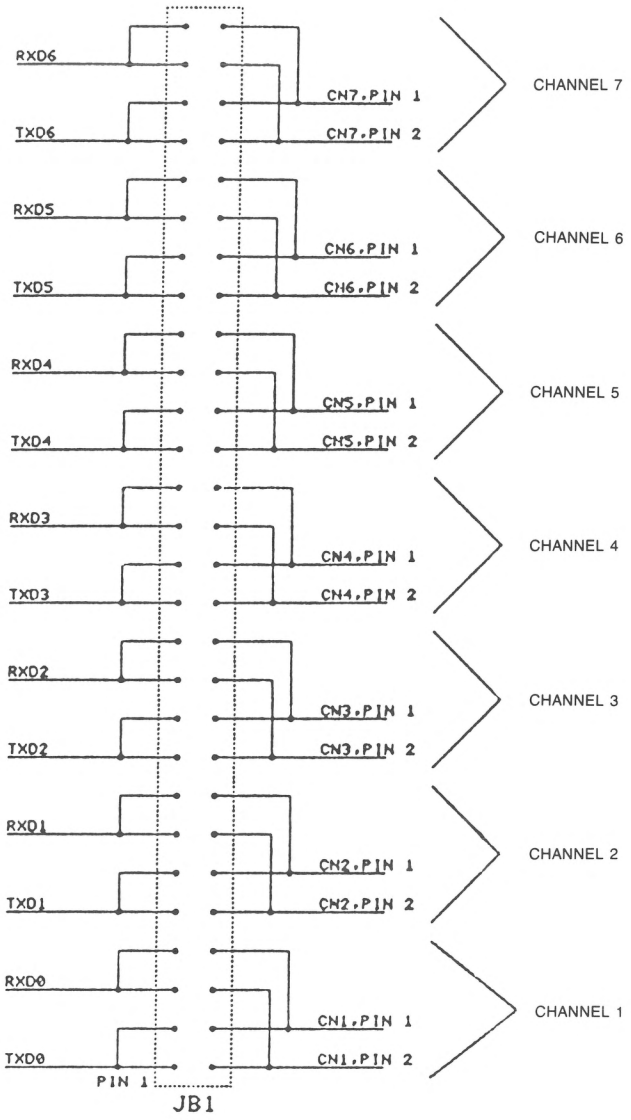


FIGURE 1 — JUMPER BLOCK SCHEMATIC

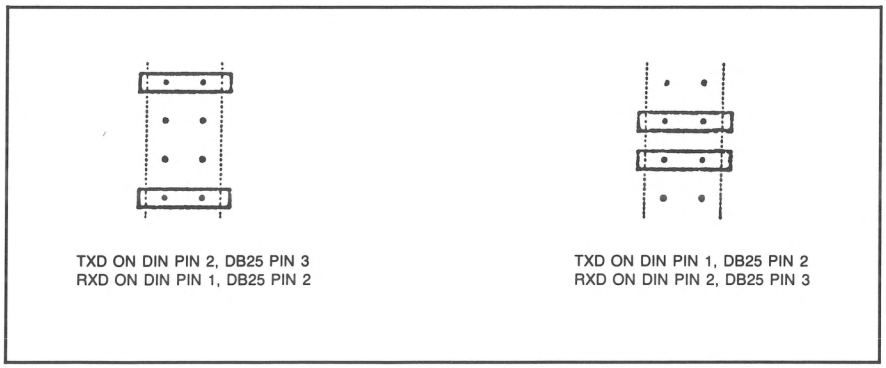


FIGURE 2 — OPTIONS FOR CONNECTING TXD & RXD FOR EACH CHANNEL

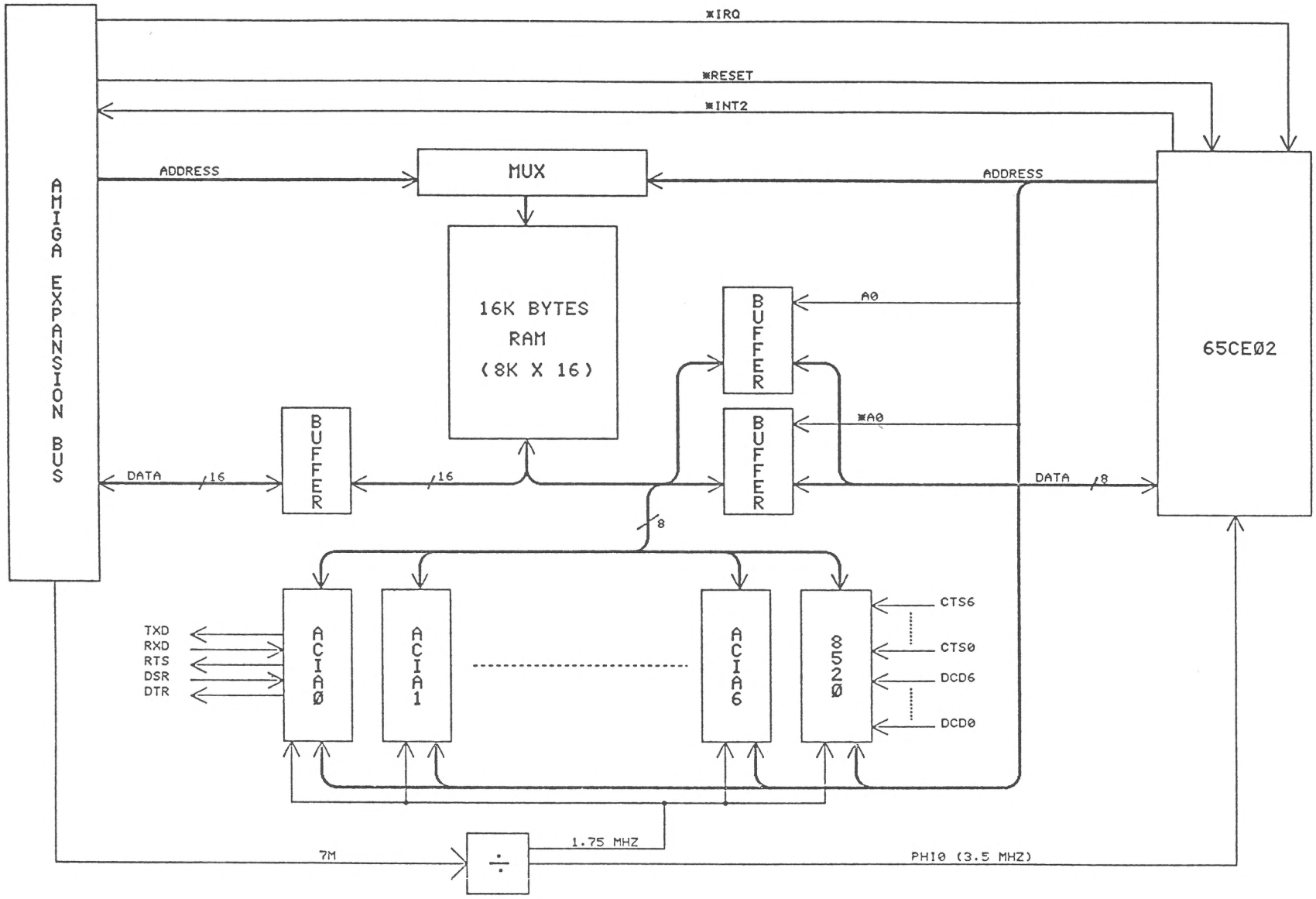


FIGURE 3 — A2232 SYSTEM BLOCK DIAGRAM

board offset	description
$0000-$3FFF	16k bytes of shared RAM
$4000	reset the *INT2 interrupt caused by the 6502
$8000	set 6502's *RESET line low
$A000	set 6502's *IRQ line low
$C000	set 6502's *RESET line high

AMIGA's MEMORY MAP OF A2232

The control signals listed above are affected when the Amiga does an access (read or write) to the locations listed. No information is passed over the data bus.

The 6502 executes code which is downloaded by the Amiga into shared RAM. When the Amiga goes through a hardware reset, the *RESET line to the 6502 is latched low, keeping it frozen. This gives the Amiga a chance to download the code which the 6502 is to execute. After the code is downloaded, the 6502 is started when the Amiga does a dummy access at board offset of $C000, allowing the *RESET line to go high. The Amiga can freeze the 6502 at any time later by accessing location $8000, latching the *RESET line low again. More or different code may now be loaded, and the 6502 restarted again.

The 6502 has control over all 7 of the 6502 ACIAs. The Amiga cannot access them directly.

address	description
$0000-$3FFF	16k bytes of shared RAM
$4400	ACIA for channel 1
$4C00	ACIA for channel 2
$5400	ACIA for channel 3
$5C00	ACIA for channel 4
$6400	ACIA for channel 5
$6C00	ACIA for channel 6
$7000	set Amiga's *INT2 interrupt low
$7400	ACIA for channel 7
$7C00	8520 CIA
$8000	Reset (set high) the *IRQ caused by the Amiga
$C000-$FFFF	16k bytes of shared RAM

6502's MEMORY MAP OF THE A2232

Note that 16k of RAM appears to the 6502 in 2 places. This was done so that the 6502's 'zero page' of memory and the reset vectors could be handled with the same RAM.

A2232 System Timing

The 7 Megahertz clock coming from the Amiga is used to drive a state machine that generates the clocks used on the A2232. The PHI0 clock which drives the 6502 is divided down from the 7M clock. Normally, the 6502 runs at 3.5 Mhz. However, so that the board can use the less expensive 2 Mhz 6551's, the 6502 must slow down to 1.75 Mhz when accessing the ACIA's (6551's). Since the 6551's are provided with a constant 1.75 Mhz clock, the 6502 must first sync up with the 6551's clock before completing the access. The 6502 is also slowed down while the Amiga accesses the shared RAM. This is done by keeping the PHI0 clock low while the 68000 accesses the RAM, effectively halting the 6502.

Figure 4 illustrates the operation of the state machine. Each of the states is 1 7M cycle long (140 nanosecs). The arrows connecting each of the states are numbered as different transitions.

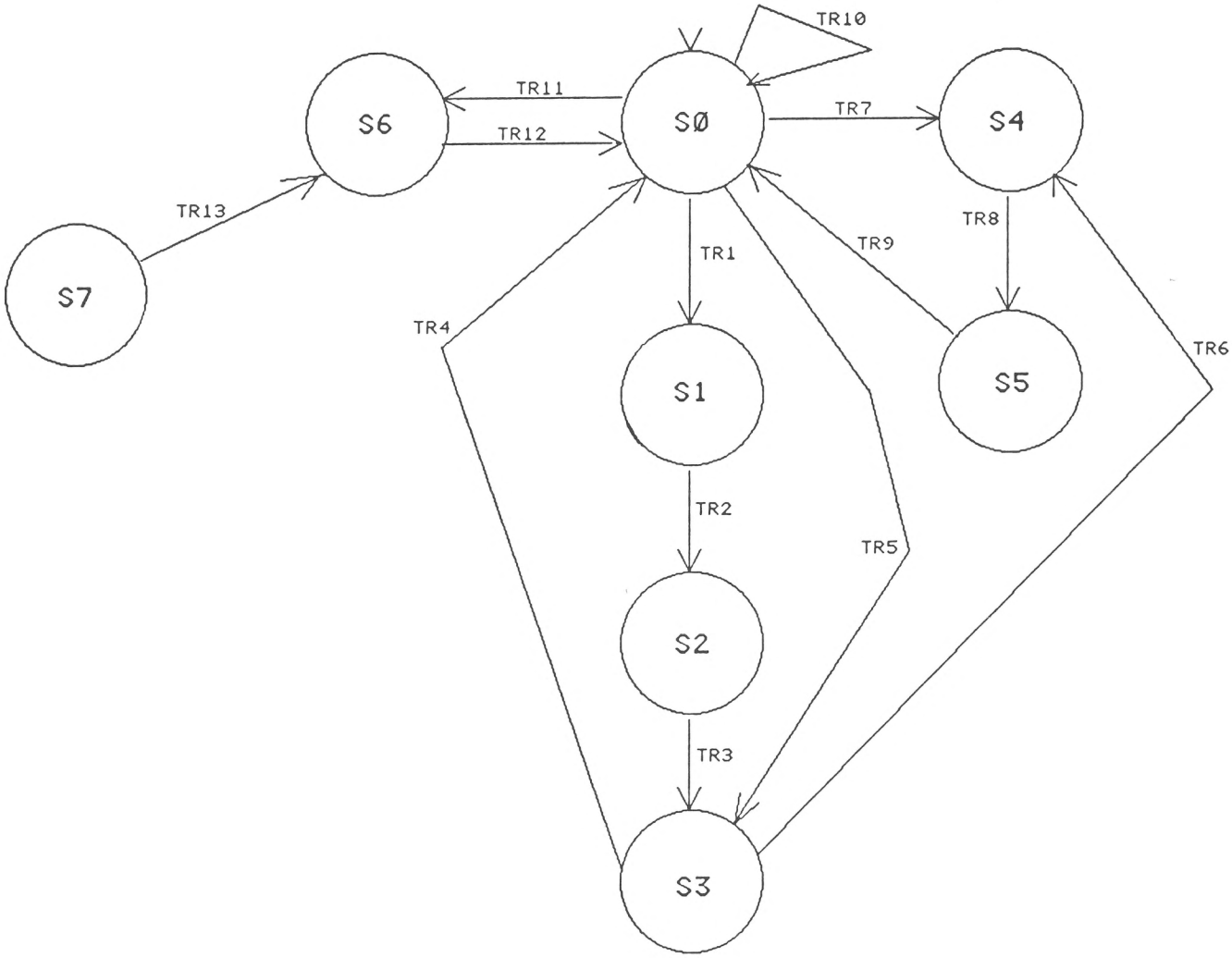


FIGURE 4 — A2232 STATE MACHINE DIAGRAM

6502 RAM ACCESS

The 6502 accesses ram during states S0 and S3. If it is determined during S0 that the 6502 wants to access the RAM, TR5 is used, bypassing S1-S2. The Phi0 clock is low during S0, and goes high during S3, yielding the 3.5 Mhz clock. At the end of S3, there are 2 different transitions that can be taken. TR4 is taken if the 68000 is not waiting to access the RAM. If the 68000 is waiting to get at the RAM, but is not properly synched with the C1 clock, TR4 is also taken. TR6 is taken when the 68000 is waiting, and is properly synched.

Referring to figure 5 ...

(7) read data setup time : >= 40 nsecs

280	Phi2 cycle time
− 50	6502 address setup time (max)
− 15	74F257 delay (max)
− 15	*CS goes low, 20L8B delay (max)
−100	RAM access time
− 18	74LS245 delay (max)
82	

(8) read data hold time : >= 10 nsecs

5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
10	

(10) write data setup time : >= 50 nsecs

140	Phi2 high time
− 50	6502 write data delay (max)
− 18	74LS245 delay (max)
− 30	Phi0 to Phi2 delay (max)
+ 5	20L8B PAL delay (min)
47	

(11) write data hold time : >= 5 nsecs

5	Phi0 to Phi2 delay (min)
+ 5	20L8 PAL delay (min)
+ 5	74LS245 turn off (min)
15	

6502 ACCESSING 6551's

Since the 6551's can only run at 1.75 Mhz, they must be provided with a constant 1.75 Mhz (or less) clock. In order for the 6502 to access the 6551, it must slow down to this speed as well. During S0, the state machine determines that the 6502 wants to access a 6551. If the clock driving the 6551 is currently low, then the 6502 is in sync with the 6551 (the PHI0 clock is always low during S0). TR1 is taken and the access may continue. If the 6551 clock is high, then they are out of sync, and TR11 is taken. TR12 immediately follows TR11, during which the 6551 clock is inverted. The state machine now determines during S0 that they are in sync, and TR1 can be taken. PHI0 and the 6551 clock are both low during S1, and go high during S2 and S3, yielding 1.75 Mhz. At the end of S3 the same decisions as described at the end of a RAM access are again executed.

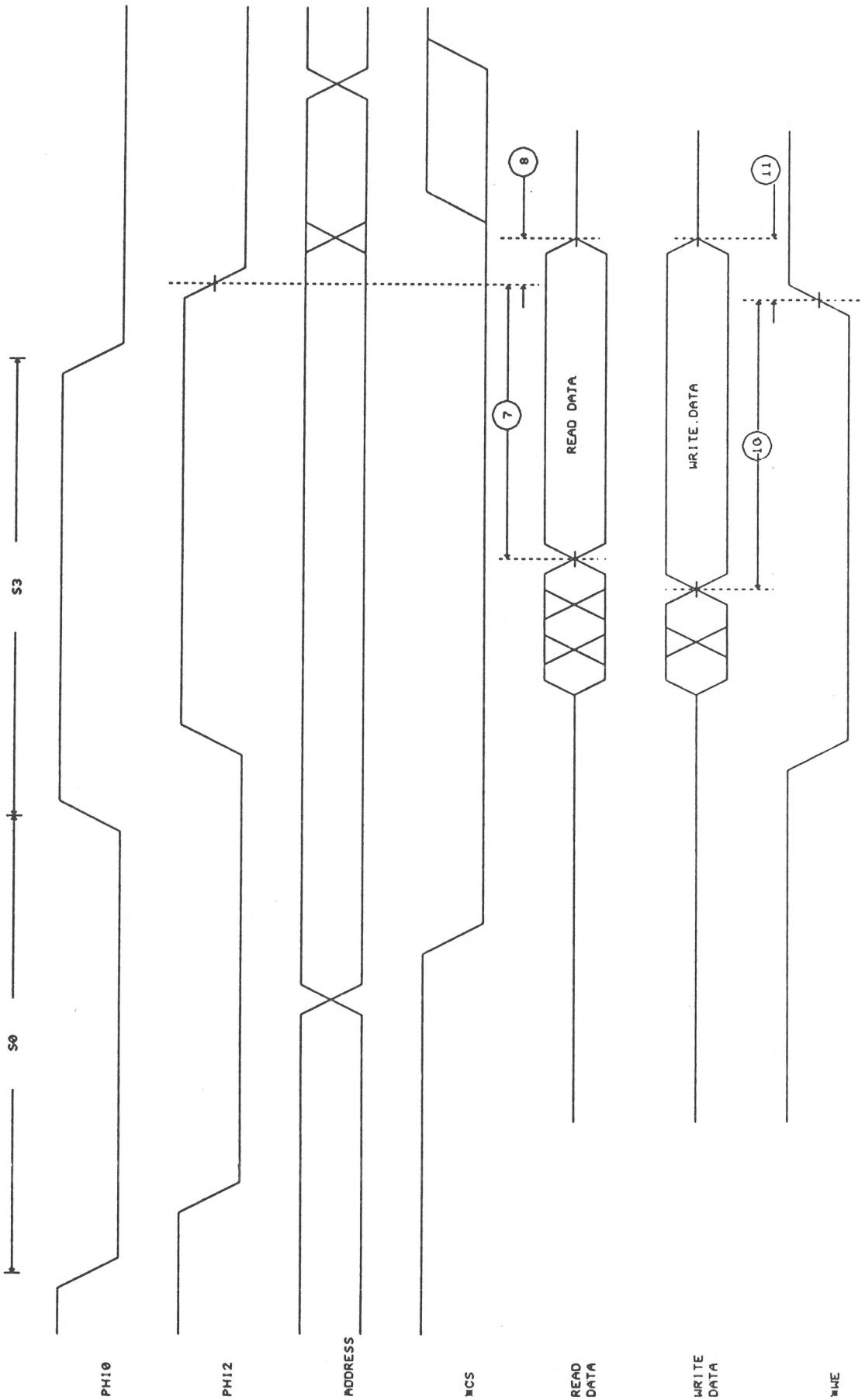


FIGURE 5 — 6502 RAM ACCESS

Referring to figure 6 ...

(1) setup time for ADR, RSO-3,R/W,CS,*CS : > = 70 nsecs

The latest of these signals is *CS.

280	6551 CLK low time
− 30	Phi0 to Phi2 delay (max)
− 40	6502 Address setup time (max)
− 30	74LS138 delay (max)
180	

(2) write data setup time : > = 60 nsecs

280	6551 CLK high time
− 30	Phi0 to Phi2 delay (max)
− 50	6502 write data setup time (max)
− 18	74LS245 delay (max)
182	

(3) write data hold time : > = 20 ns

5	Phi0 to Phi2 delay (min)
+ 5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
15	(case 1)
5	Phi0 to Phi2 delay (min)
+ 5	6502 write data hold (tHD min)
+ 5	74LS245 in to out delay (min)
15	(case 2)

(4) read data setup time : > = 40 nsecs

280	Phi2 high time
+ 5	Phi0 to Phi2 delay (min)
−150	read data access of 6551 (max)
− 18	74LS245 delay (max)
107	

(5) read data hold time : > = 10 nsecs

5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
10	

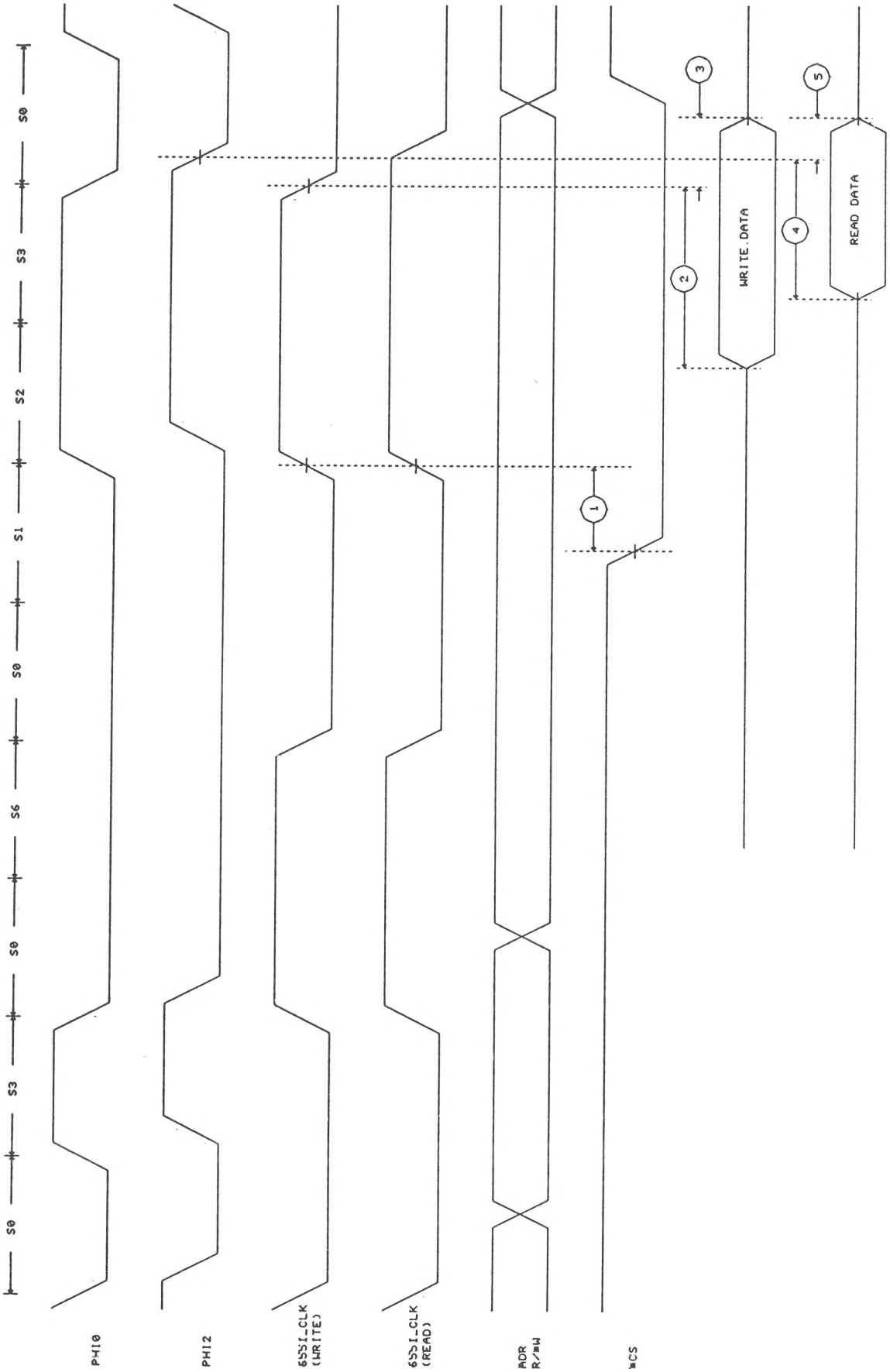


FIGURE 6 — ACCESSING 6551's

68000 RAM ACCESS

There are 2 states during which a 68000 request can be recognized. One of these is S3, which has already been described. During S0 a 68000 request can also be recognized. In both instances, the 68000 takes precedence. If the 68000 doesn't want access, then the 6502 is allowed to continue. During 68000 accesses the 6502 is halted by holding the Phi0 clock low. TR7 and TR6 both bring the state machine to S4, where the 68000 access is allowed to finish. From the time that the board is selected, it drives the override (*OVR) and *DTACK signals until the end of S5. As long as it may take for the state machine to get to S4, wait states are inserted into the 68000 access by keeping *DTACK high. At the beginning of S4 *DTACK goes low signalling to the 68000 that the access may be completed.

Referring to figure 7 ...

(15) read data setup time : > = 10 nsecs

referenced from the start of 68000 T4 ...

210	time from start of T4 to end of T6
− 15	Q delay of 16R8A PAL, Phi0 goes low (max)
− 30	Phi0 to Phi2 delay (max)
− 15	20L8B PAL delay, MUX goes low (max) (*RAMCS goes low too)
− 15	74F257 switching delay (max)
− 100	RAM access time
− 10	74ALS245 delay (max)
− 18	74LS245 delay, on expansion bus (max)
7	

(16) read data hold time : > = 0

Obvious.

(17) write data setup time : > = 50 nsecs

Assume that C3 transitions coincident with the rising edge of the 7M clock. Referenced from the rising C3 at the beginning of T4, the RAM *WE goes high 140 ns later. Referenced from the same rising edge of C3, the data becomes valid:

15	Q delay of 16R8A PAL (max)
+ 35	20L8 PAL delay (max)
+ 7	74F32 delay (max)
+ 20	74ALS245 turn on time (max)
77 ns	

So, 140 − 74 = 66 ns

(18) write data hold time : > = 5 nsecs

The write pulse went away half way through S5. The data and addresses stay valid through the rest of S5, or approximately 70 nsecs.

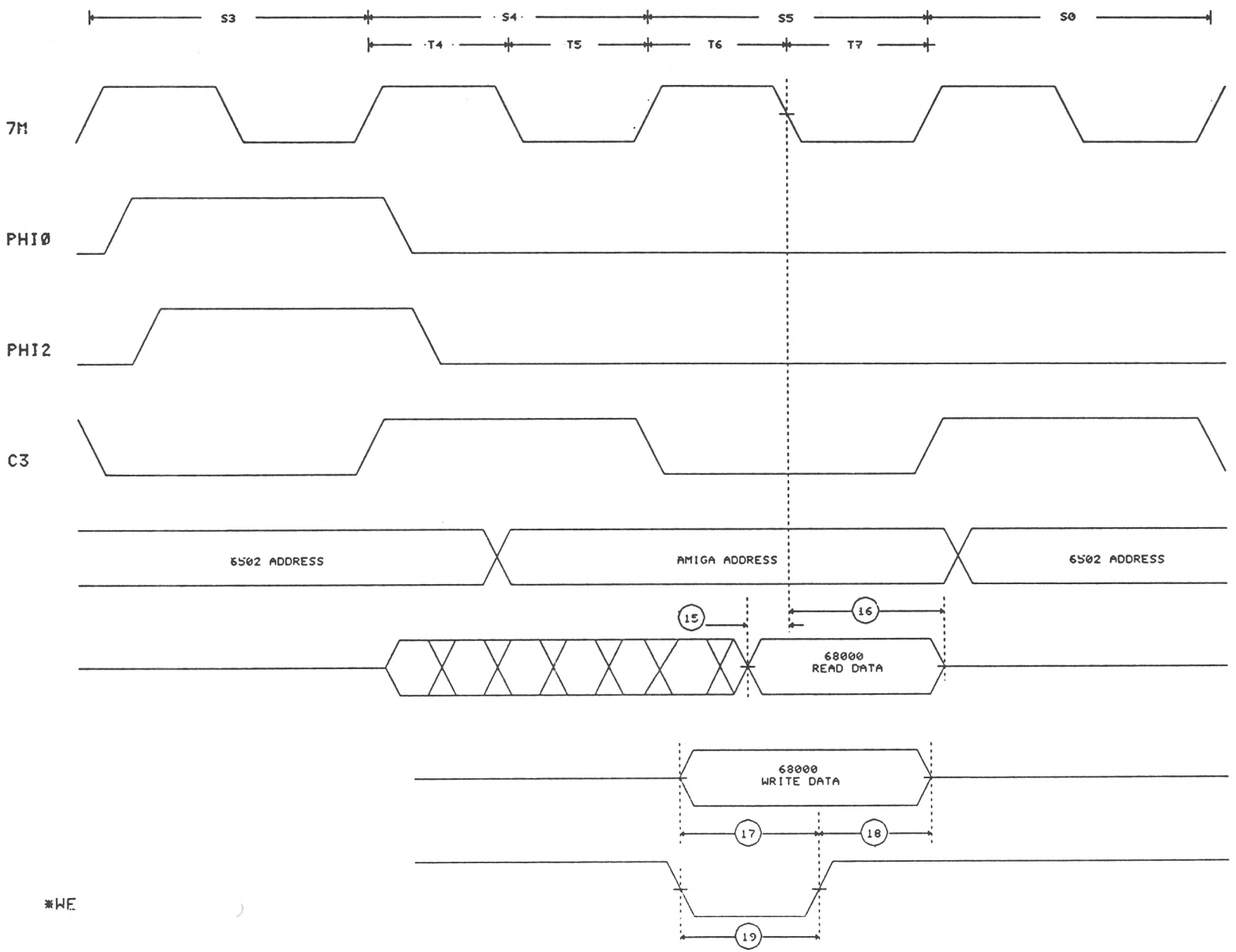


FIGURE 7 — 68000 RAM ACCESS

Commodore International Spare Parts List
SHIPPING ASSEMBLIES

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

312859-01	A2232 SHIPPING ASSY (U.S.)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
314877-04	BOOKLET SERVICE CENTER LIST
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7)
318290-01	CARD WARRANTY U.S.
318928-01	BAG ANTI STATIC
318896-01	S/W LICENSE AGREEMENT
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM
312341-02	CARD DISK EXCHANGE

312859-02	A2232 SHIPPING ASSY (EFIGS)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7) (CAN SUB to −01)
318928-01	BAG ANTI STATIC
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM

312859-03	A2232 SHIPPING ASSY (CANADA)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7)
318882-01	CARD WARRANTY CANADA
318928-01	BAG ANTI STATIC
318896-01	S/W LICENSE AGREEMENT
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM
318556-02	CARD DISK EXCHANGE CANADA

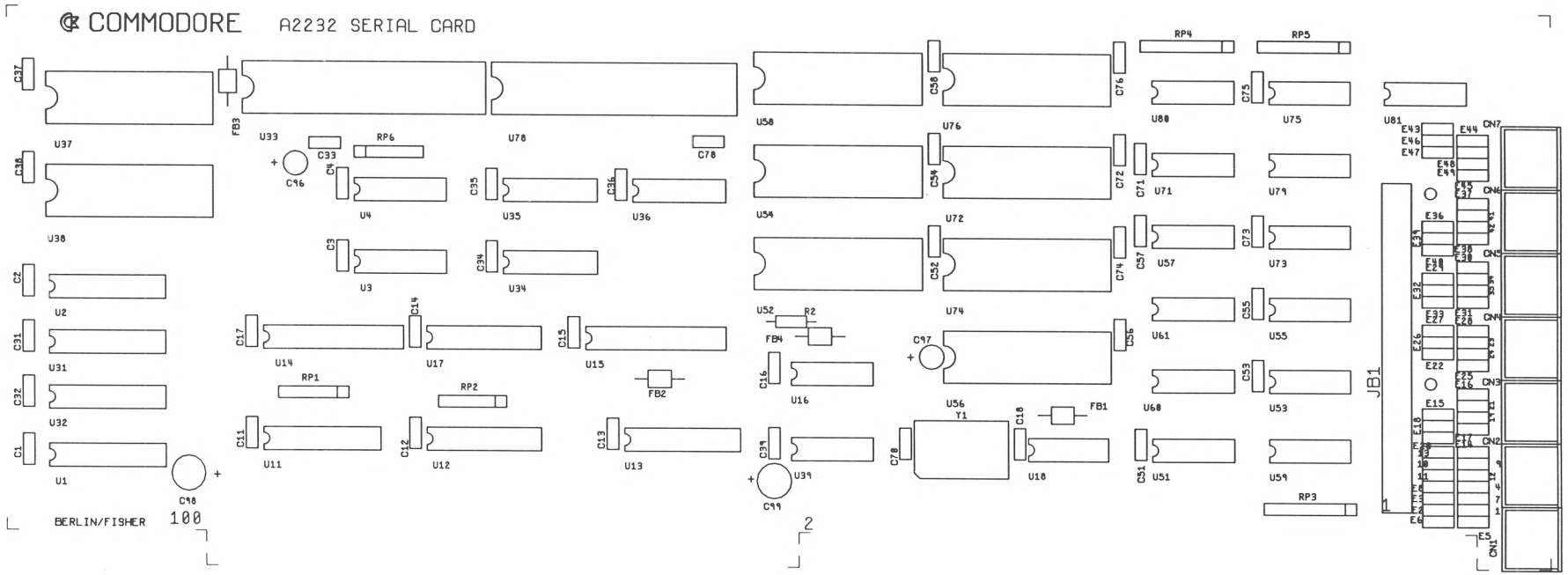
312859-04	A2232 SHIPPING ASSY (AUSTRALIA)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7)
318884-01	CARD WARRANTY AUSTRALIA
318928-01	BAG ANTI STATIC
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM

Commodore International Spare Parts List
PCB Components
PCB Assembly #311611-01

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

IC COMPONENTS		
312860-01	PCB ASSY A2232 SERIAL CARD	
318029-03	8520A-1	U78
390373-01	16R8A PAL	U13
390370-02	16L8 PAL	U17
390371-02	20L8A PAL	U15
390372-03	20L8B PAL	U14
901521-06	74LS74	U18
901522-30	7407	U39
390077-01	74F32	U16
318041-01	74F521	U12
901521-16	74LS138	U36
901521-46	74LS245	U31,U32
390091-01	74F257	U3,U4,U34,U35
901521-29	74LS373	U11
318092-01	74ALS245	U1,U2
901882-01	MC1488 QUAD DRIVER	U59-U61,U79-U81
901883-01	MC1489 QUAD RECEIVER	U51,U53,U55,U57,U71, U73,U75
901895-03	6551A UART	U52,U54,U56,U58,U72, U74,U76
310024-02	8K X 8 SRAM 100 NS	U37,U38
390375-02	LSI CPU 65CE02	U33
901895-02	6551A UART	SUB FOR ITEM 21
SOCKETS		
904150-08	20 PIN DIP	U13,U17
390060-01	24 PIN DIP SOCKET	U14,U15
904150-05	28 PIN DIP	U52,U54,U56,U58,U72, U74,U76
904150-06	40 PIN DIP	U33,U78

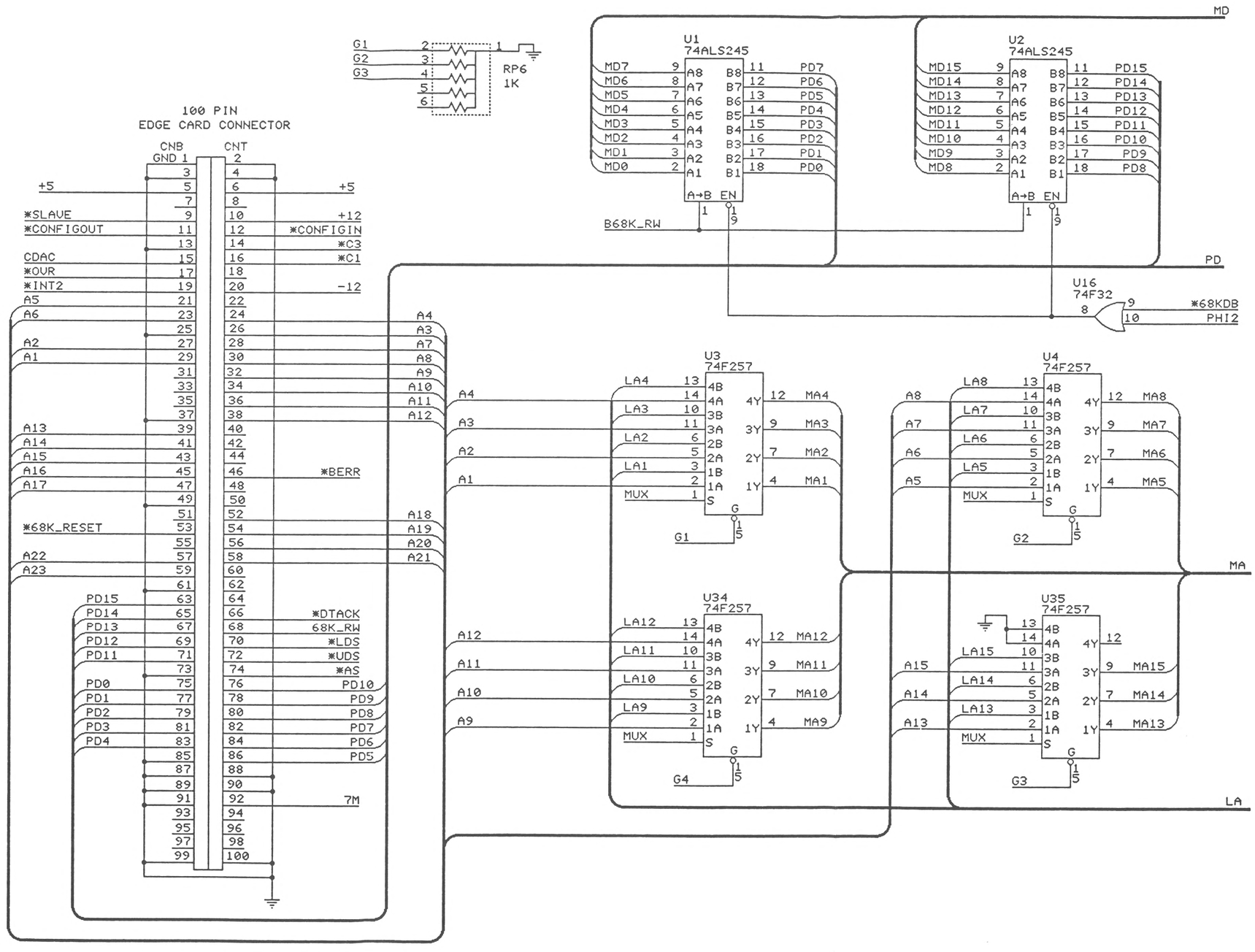
RESISTORS		
902441-22	PAK 6 PIN SIP 1K	RP1,RP6
902441-31	PAK 6 PIN SIP 4.7K	RP2
902442-55	PAK 8 PIN SIP 4.7K	RP3-RP5
901550-01	1K 5% ¼ WATT	R2
901550-18	2.2K 5% ¼ WATT	R3,R4
CAPACITORS		
900020-01	.1 UF –50V 20%	C1-C4,C11-C18,C31-C39, C51-C58,C70-C76,C78
390101-05	ELECT ALUM RAD LEAD 4.7 UF	C96-C99
MISCELLANEOUS		
325566-16	OSCILLATOR 1.8432 MHZ	Y1
251842-04	EMI FILTER 470PF	EMI 1-EMI 49
903025-01	FERRITE BEAD	FB1-FB4
903345-29	CONN 56 PIN DIL HEADER .10 CENTERS	JB1
390043-01	SHUNT FEMALE 2 POS	
390218-02	CONN 8 PIN MINI DIN RECEPTACLE	CN1-CN7
312865-01	EXTENSION CARD PANEL	
906800-05	SCREW 3M X 6 LG PAN HEAD PHILLIPS - QTY 2	
316914-01	LABEL FCC ID A2232	

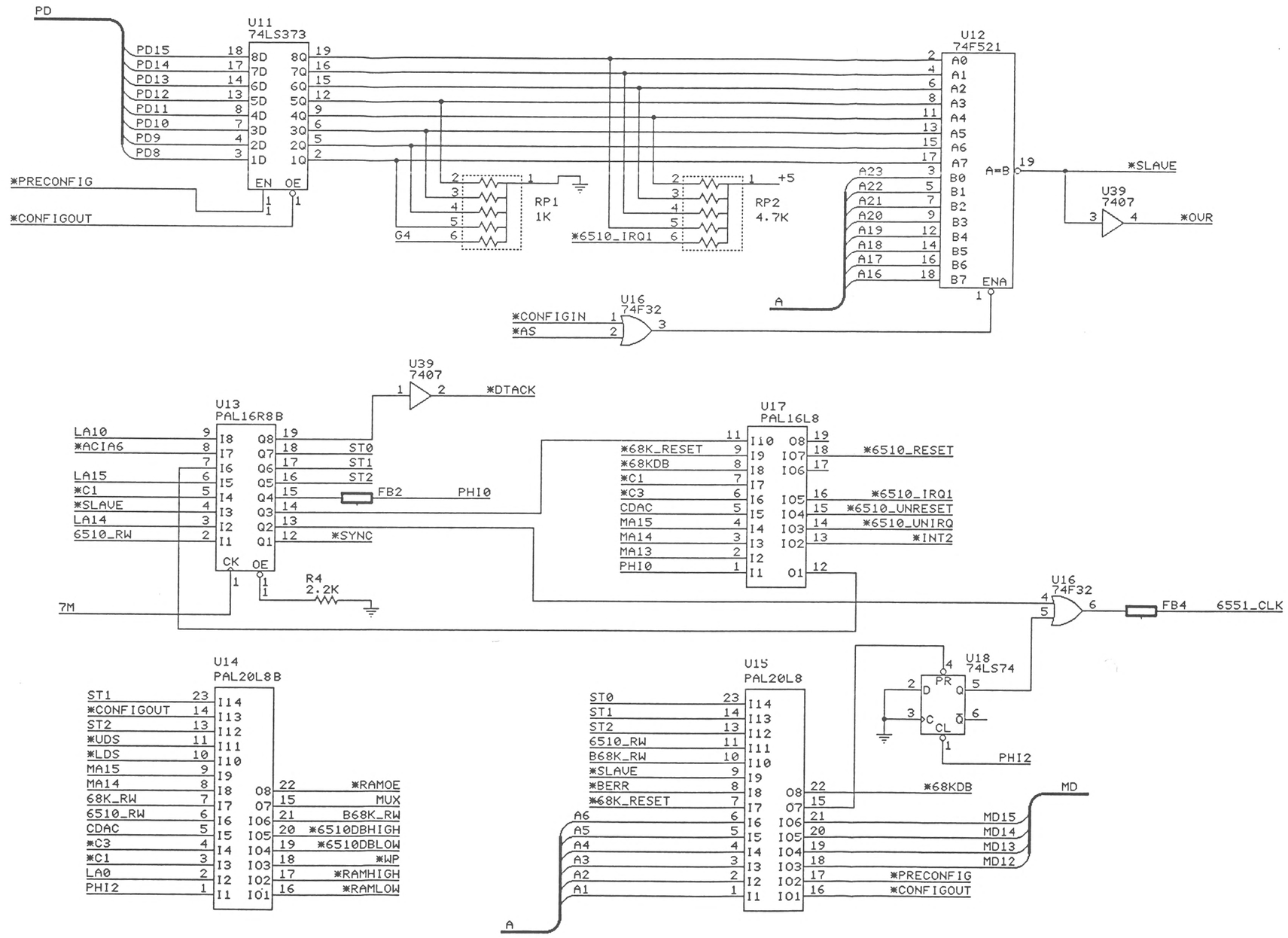


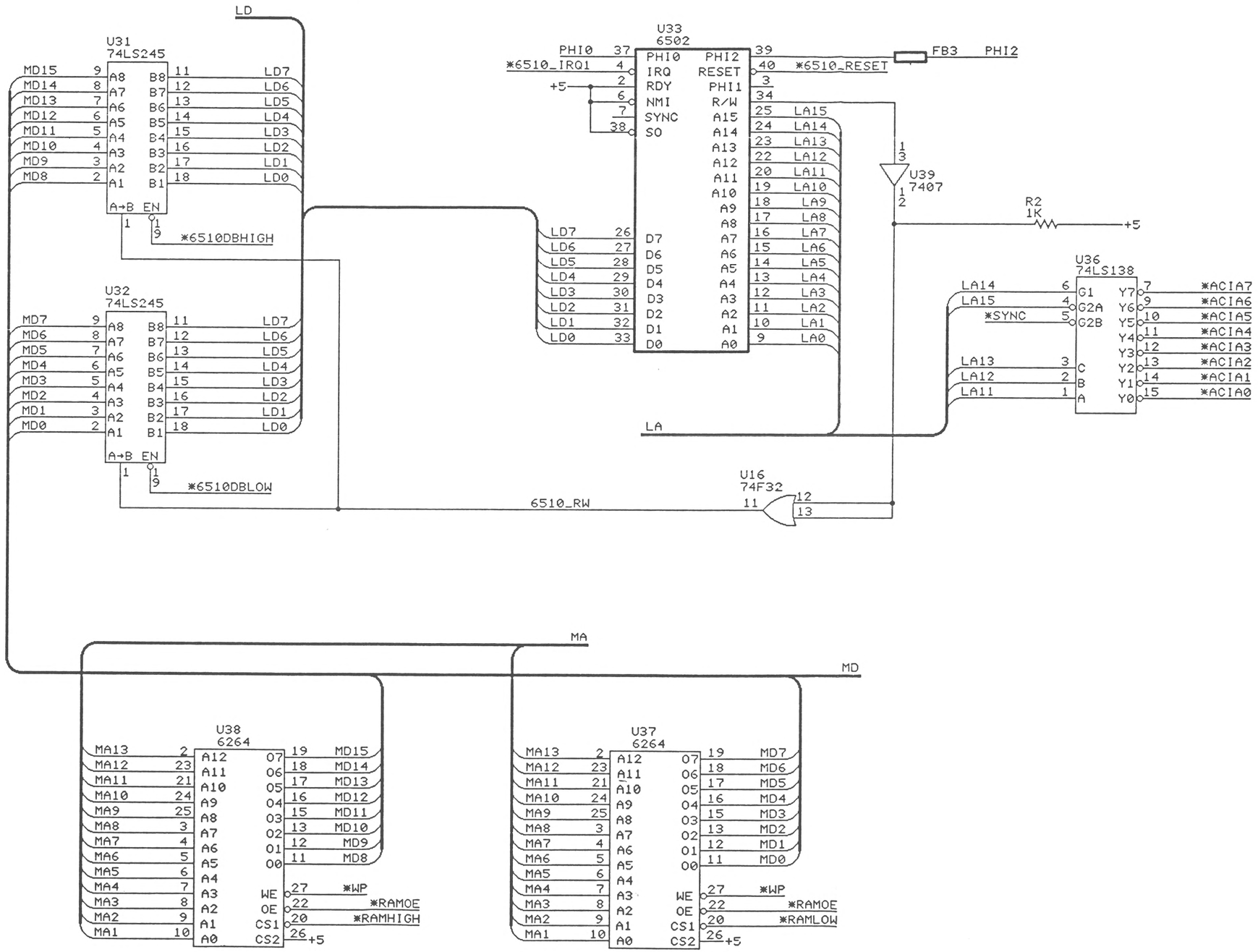
PCB BOARD LAYOUT #312863, REV. 5

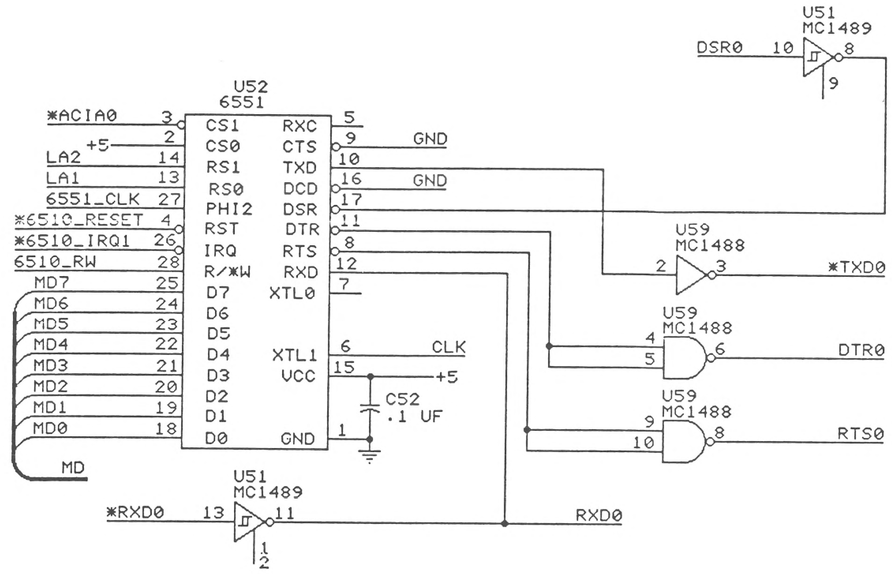
A2232 SCHEMATIC #312861, REV. A — SCHEMATIC PAGE INDEX

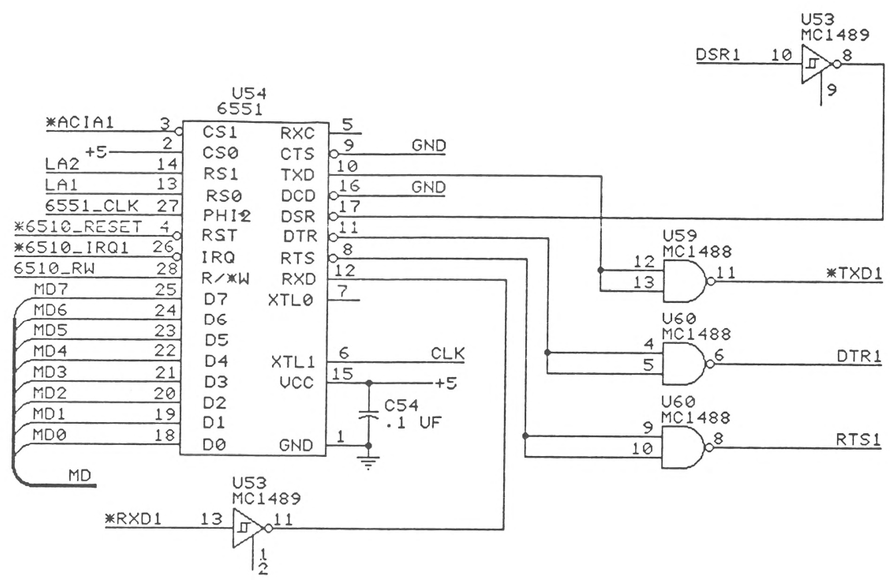
Sheet 1 of 8

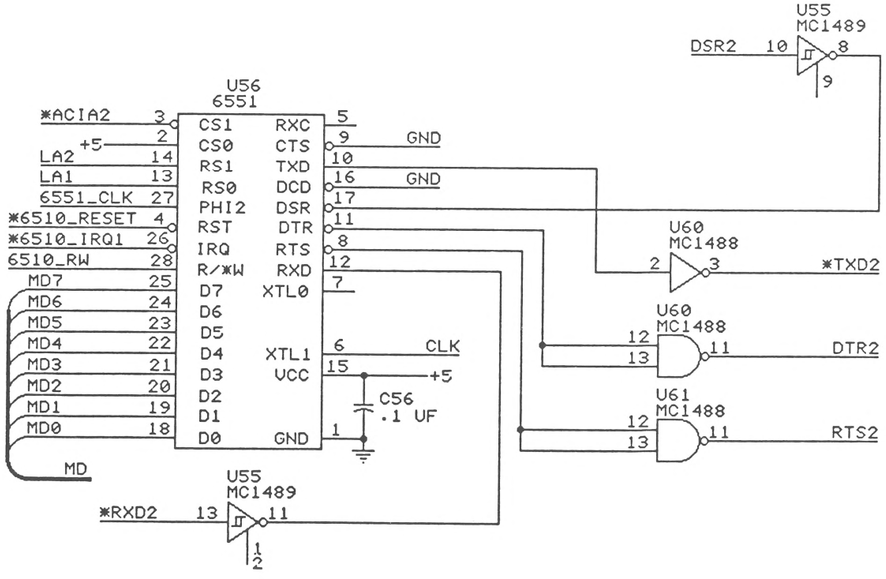

100 PIN
EDGE CARD CONNECTOR
CNB
CNT
GND 1
2
3
4
+5
5
6
+5
7
8
*SLAVE
9
10
+12
*CONFIGOUT
11
12
*CONFIGIN
13
14
*C3
CDAC
15
16
*C1
*OUR
17
18
*INT2
19
20
-12
A5
21
22
A6
23
24
A4
25
26
A3
A2
27
28
A7
A1
29
30
A8
31
32
A9
33
34
A10
35
36
A11
37
38
A12
A13
39
40
A14
41
42
A15
43
44
A16
45
46
*BERR
A17
47
48
49
50
*68K_RESET
51
52
A18
53
54
A19
55
56
A20
A22
57
58
A21
A23
59
60
61
62
PD15
63
64
PD14
65
66
*DTACK
PD13
67
68
68K_RW
PD12
69
70
*LDS
PD11
71
72
*UDS
73
74
*AS
PD0
75
76
PD10
PD1
77
78
PD9
PD2
79
80
PD8
PD3
81
82
PD7
PD4
83
84
PD6
85
86
PD5
87
88
89
90
91
92
7M
93
94
95
96
97
98
99
100
RP6
1K
G1
G2
G3
MD
PD
MA
LA
U1
74ALS245
U2
74ALS245
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD15
MD14
MD13
MD12
MD11
MD10
MD9
MD8
A8
B8
A7
B7
A6
B6
A5
B5
A4
B4
A3
B3
A2
B2
A1
B1
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
PD15
PD14
PD13
PD12
PD11
PD10
PD9
PD8
A→B
EN
B68K_RW
U16
74F32
*68KDB
PHI2
U3
74F257
U4
74F257
U34
74F257
U35
74F257
LA4
LA3
LA2
LA1
LA8
LA7
LA6
LA5
LA12
LA11
LA10
LA9
LA15
LA14
LA13
MUX
4B
4A
3B
3A
2B
2A
1B
1A
S
G
4Y
3Y
2Y
1Y
MA4
MA3
MA2
MA1
MA8
MA7
MA6
MA5
MA12
MA11
MA10
MA9
MA15
MA14
MA13

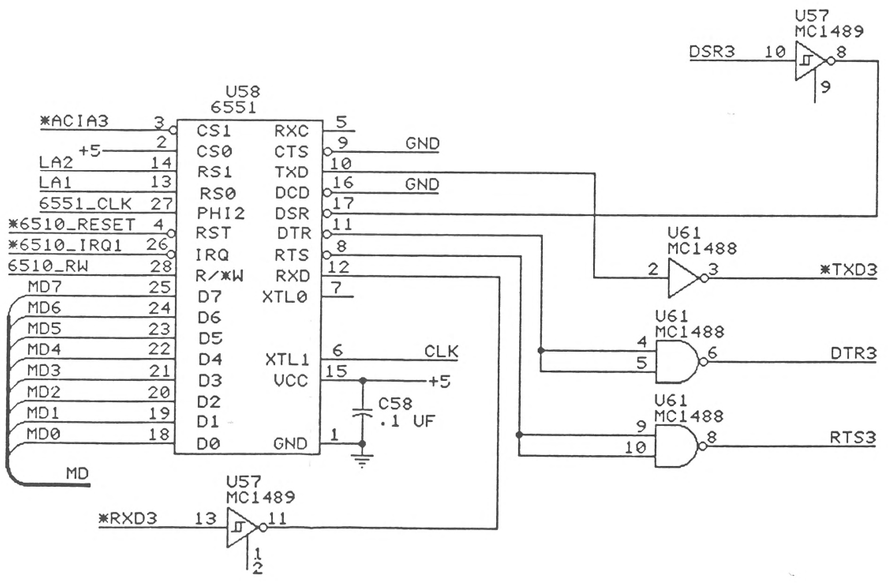

PD
U11
74LS373
PD15
PD14
PD13
PD12
PD11
PD10
PD9
PD8
8D
7D
6D
5D
4D
3D
2D
1D
8Q
7Q
6Q
5Q
4Q
3Q
2Q
1Q
EN
OE
*PRECONFIG
*CONFIGOUT
G4
RP1
1K
*6510_IRQ1
RP2
4.7K
+5
U12
74F521
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
A=B
ENA
A23
A22
A21
A20
A19
A18
A17
A16
A
*SLAVE
U39
7407
*OUR
U16
74F32
*CONFIGIN
*AS
U39
7407
*DTACK
U13
PAL16R8B
LA10
*ACIA6
LA15
*C1
*SLAVE
LA14
6510_RW
ST0
ST1
ST2
FB2
PHI0
*SYNC
CK
OE
R4
2.2K
7M
U17
PAL16L8
*68K_RESET
*68KDB
*C1
*C3
CDAC
MA15
MA14
MA13
PHI0
*6510_RESET
*6510_IRQ1
*6510_UNRESET
*6510_UNIRQ
*INT2
U16
74F32
FB4
6551_CLK
U18
74LS74
PR
D
C
CL
Q
PHI2
U14
PAL20L8
ST1
*CONFIGOUT
ST2
*UDS
*LDS
MA15
MA14
68K_RW
6510_RW
CDAC
*C3
*C1
LA0
PHI2
*RAMOE
MUX
B68K_RW
*6510DBHIGH
*6510DBLOW
*WP
*RAMHIGH
*RAMLOW
U15
PAL20L8
ST0
ST1
ST2
6510_RW
B68K_RW
*SLAVE
*BERR
*68K_RESET
A6
A5
A4
A3
A2
A1
A
*68KDB
MD
MD15
MD14
MD13
MD12
*PRECONFIG
*CONFIGOUT

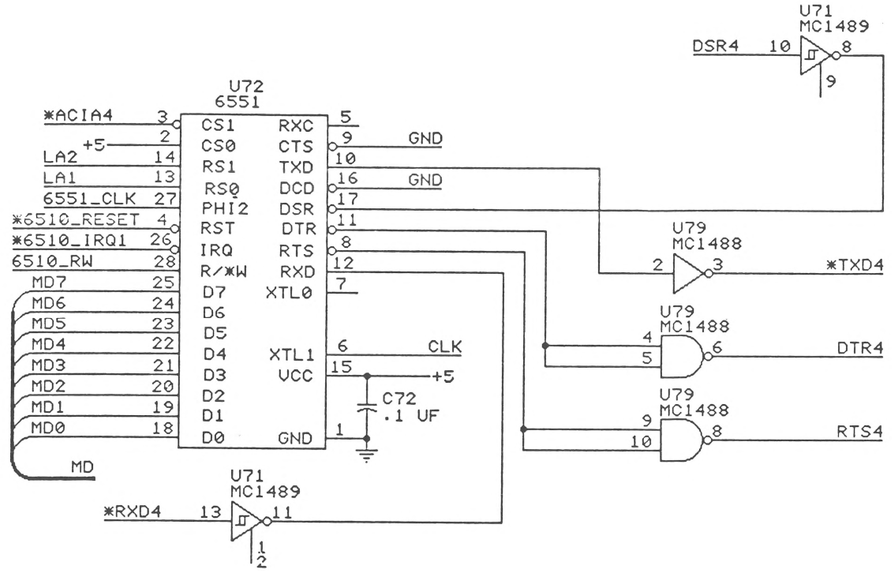

LD
U31
74LS245
MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8
A8 A7 A6 A5 A4 A3 A2 A1
B8 B7 B6 B5 B4 B3 B2 B1
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
A→B EN
*6510DBHIGH
U32
74LS245
MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0
*6510DBLOW
U33
6502
PHI0 *6510_IRQ1 +5
IRQ RDY NMI SYNC SO
PHI2 RESET PHI1 R/W
*6510_RESET
FB3 PHI2
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
D7 D6 D5 D4 D3 D2 D1 D0
LA15 LA14 LA13 LA12 LA11 LA10 LA9 LA8 LA7 LA6 LA5 LA4 LA3 LA2 LA1 LA0
LA
U39
7407
R2
1K
+5
U36
74LS138
LA14 LA15 *SYNC
LA13 LA12 LA11
G1 G2A G2B
C B A
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
*ACIA7 *ACIA6 *ACIA5 *ACIA4 *ACIA3 *ACIA2 *ACIA1 *ACIA0
U16
74F32
6510_RW
MA
MD
U38
6264
MA13 MA12 MA11 MA10 MA9 MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
07 06 05 04 03 02 01 00
MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8
WE OE CS1 CS2
*WP *RAMOE *RAMHIGH +5
U37
6264
MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0
*WP *RAMOE *RAMLOW +5

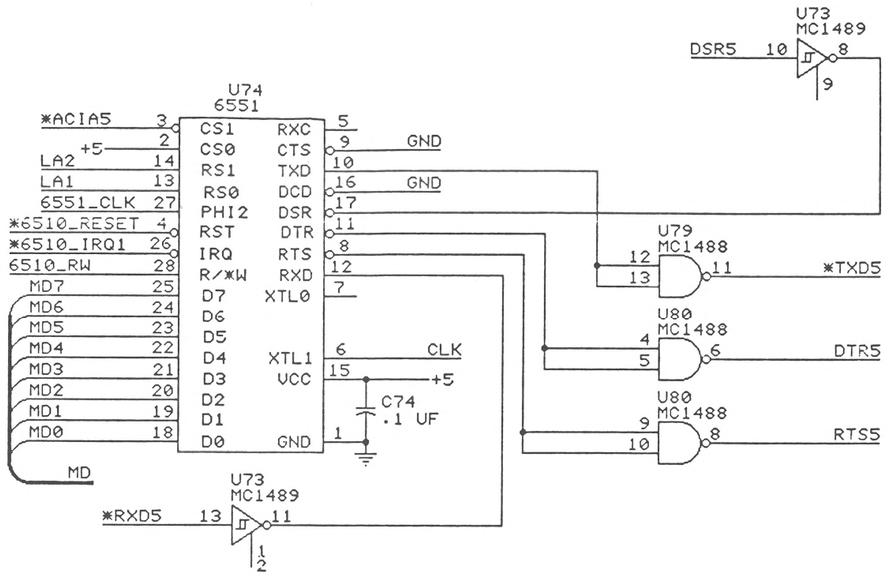

U52
6551
*ACIA0
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
CLK
C52
.1 UF
U51
MC1489
DSR0
U59
MC1488
*TXD0
DTR0
RTS0
*RXD0
RXD0

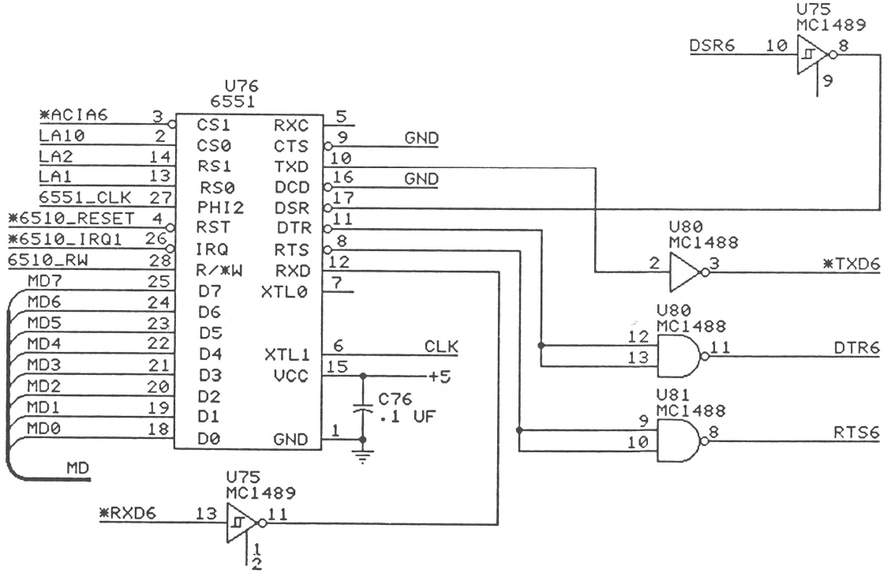

U54
6551
*ACIA1
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
CLK
C54
.1 UF
U53
MC1489
DSR1
U59
MC1488
*TXD1
U60
MC1488
DTR1
RTS1
*RXD1

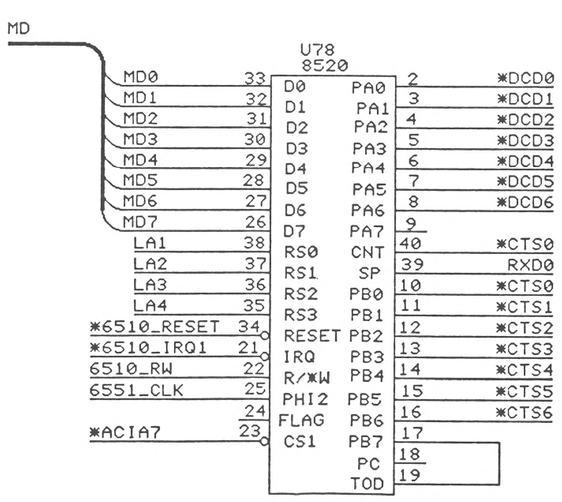

U56
6551
*ACIA2
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
CLK
C56
.1 UF
U55
MC1489
DSR2
U60
MC1488
*TXD2
DTR2
RTS2
*RXD2

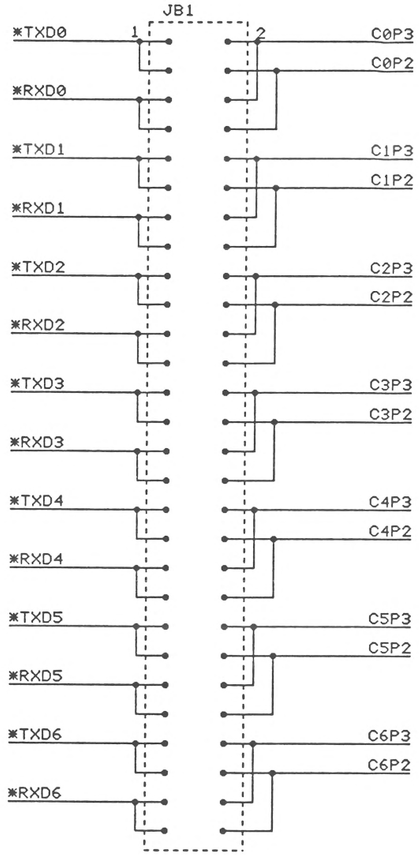

U58
6551
*ACIA3
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
CLK
C58
.1 UF
U57
MC1489
DSR3
U61
MC1488
*TXD3
DTR3
RTS3
*RXD3

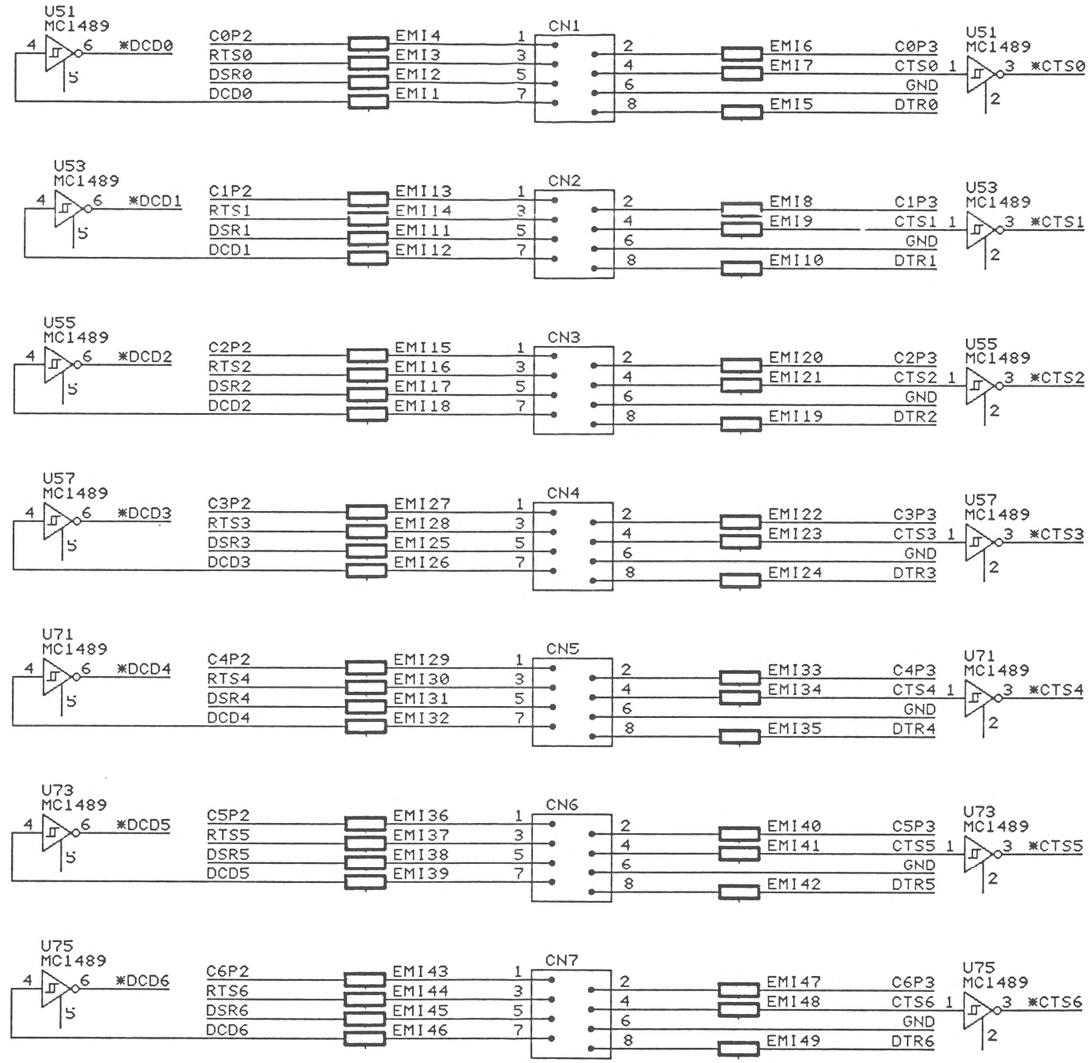

U72
6551
*ACIA4
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C72
.1 UF
U71
MC1489
DSR4
*RXD4
U79
MC1488
*TXD4
DTR4
RTS4

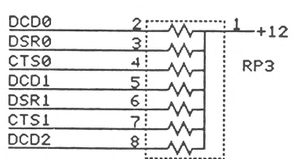

U74
6551
*ACIA5
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C74
.1 UF
U73
MC1489
DSR5
*RXD5
U79
MC1488
*TXD5
U80
MC1488
DTR5
U80
MC1488
RTS5

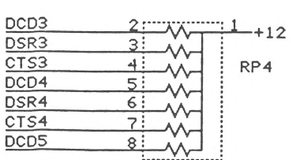

U76
6551
*ACIA6
LA10
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C76
.1 UF
U75
MC1489
DSR6
*RXD6
U80
MC1488
*TXD6
DTR6
U81
MC1488
RTS6

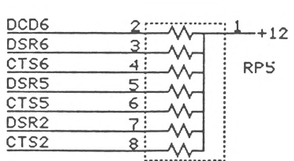

MD
U78
8520
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
LA1
LA2
LA3
LA4
*6510_RESET
*6510_IRQ1
6510_RW
6551_CLK
*ACIA7
D0
D1
D2
D3
D4
D5
D6
D7
RS0
RS1
RS2
RS3
RESET
IRQ
R/*W
PHI2
FLAG
CS1
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
CNT
SP
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC
TOD
*DCD0
*DCD1
*DCD2
*DCD3
*DCD4
*DCD5
*DCD6
*CTS0
RXD0
*CTS0
*CTS1
*CTS2
*CTS3
*CTS4
*CTS5
*CTS6

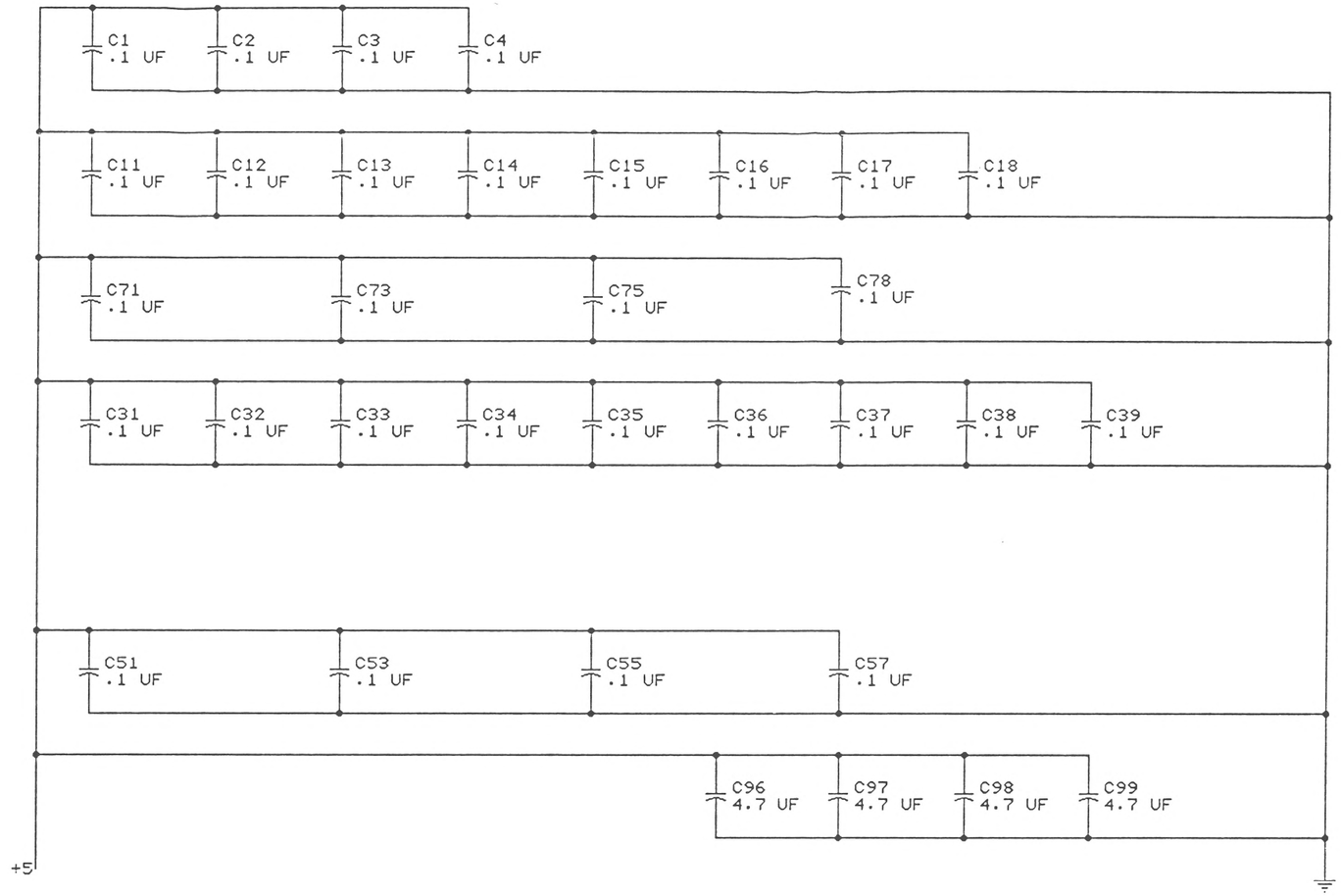

JB1
*TXD0
*RXD0
*TXD1
*RXD1
*TXD2
*RXD2
*TXD3
*RXD3
*TXD4
*RXD4
*TXD5
*RXD5
*TXD6
*RXD6
C0P3
C0P2
C1P3
C1P2
C2P3
C2P2
C3P3
C3P2
C4P3
C4P2
C5P3
C5P2
C6P3
C6P2

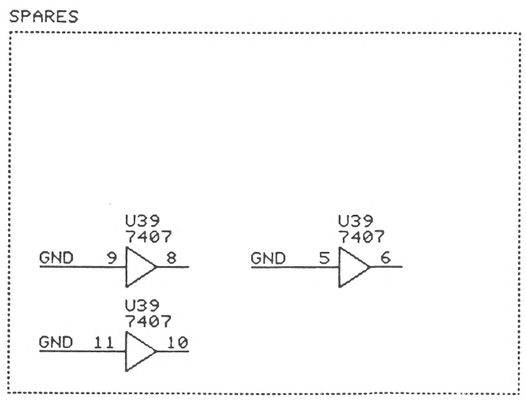

U51
MC1489
*DCD0
C0P2
RTS0
DSR0
DCD0
CN1
EMI4
EMI3
EMI2
EMI1
EMI6
EMI7
EMI5
C0P3
CTS0
GND
DTR0
*CTS0
U53
MC1489
*DCD1
C1P2
RTS1
DSR1
DCD1
CN2
EMI13
EMI14
EMI11
EMI12
EMI8
EMI9
EMI10
C1P3
CTS1
GND
DTR1
*CTS1
U55
MC1489
*DCD2
C2P2
RTS2
DSR2
DCD2
CN3
EMI15
EMI16
EMI17
EMI18
EMI20
EMI21
EMI19
C2P3
CTS2
GND
DTR2
*CTS2
U57
MC1489
*DCD3
C3P2
RTS3
DSR3
DCD3
CN4
EMI27
EMI28
EMI25
EMI26
EMI22
EMI23
EMI24
C3P3
CTS3
GND
DTR3
*CTS3
U71
MC1489
*DCD4
C4P2
RTS4
DSR4
DCD4
CN5
EMI29
EMI30
EMI31
EMI32
EMI33
EMI34
EMI35
C4P3
CTS4
GND
DTR4
*CTS4
U73
MC1489
*DCD5
C5P2
RTS5
DSR5
DCD5
CN6
EMI36
EMI37
EMI38
EMI39
EMI40
EMI41
EMI42
C5P3
CTS5
GND
DTR5
*CTS5
U75
MC1489
*DCD6
C6P2
RTS6
DSR6
DCD6
CN7
EMI43
EMI44
EMI45
EMI46
EMI47
EMI48
EMI49
C6P3
CTS6
GND
DTR6
*CTS6

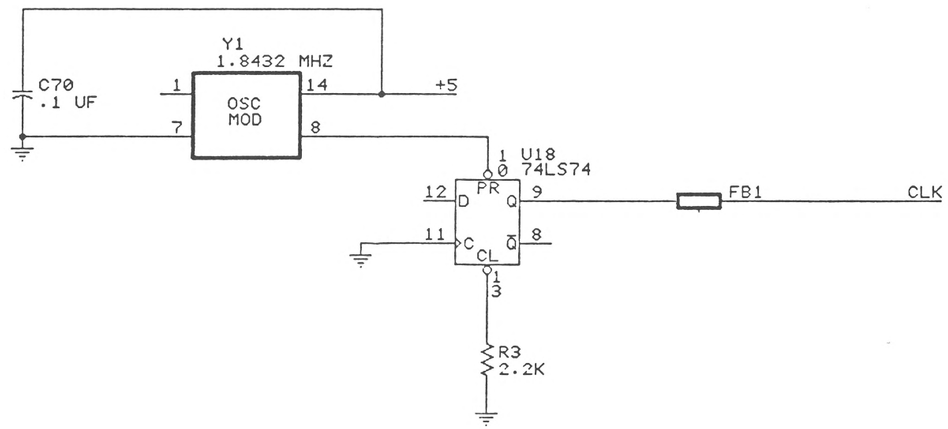

DCD0
DSR0
CTS0
DCD1
DSR1
CTS1
DCD2
+12
RP3


DCD3
DSR3
CTS3
DCD4
DSR4
CTS4
DCD5
+12
RP4


DCD6
DSR6
CTS6
DSR5
CTS5
DSR2
CTS2
+12
RP5


C1 .1 UF
C2 .1 UF
C3 .1 UF
C4 .1 UF
C11 .1 UF
C12 .1 UF
C13 .1 UF
C14 .1 UF
C15 .1 UF
C16 .1 UF
C17 .1 UF
C18 .1 UF
C71 .1 UF
C73 .1 UF
C75 .1 UF
C78 .1 UF
C31 .1 UF
C32 .1 UF
C33 .1 UF
C34 .1 UF
C35 .1 UF
C36 .1 UF
C37 .1 UF
C38 .1 UF
C39 .1 UF
C51 .1 UF
C53 .1 UF
C55 .1 UF
C57 .1 UF
C96 4.7 UF
C97 4.7 UF
C98 4.7 UF
C99 4.7 UF
+5


SPARES
U39 7407
GND 9 8
U39 7407
GND 5 6
U39 7407
GND 11 10


Y1 1.8432 MHZ
C70 .1 UF
1
7
OSC MOD
14
8
+5
U18 74LS74
PR
D
C
CL
Q
12
11
9
8
FB1
CLK
R3 2.2K